

Fig. 1

Fig. 1 is a block diagram of a digital signal processing system for a radio receiver. The system includes a phase detector (301) and a phase delaying unit (305) in a dashed box 329. The phase detector outputs signals T1, T2, T3, and T4 to a converting unit (314). The converting unit outputs signals C1, C2, C3, and C4 to a series of eight component ROMs (317, 321, 318, 322, 319, 323, 320, 324). Each ROM outputs to a summing junction (325, 326). The summing junctions output to a judging unit (327). A clock generating unit (328) provides a clock signal to the symbol section detecting unit (333) and the PLL unit (334). The symbol section detecting unit (333) outputs to the judging unit (327). The PLL unit (334) outputs to the clock generating unit (328). The system is divided into three dashed boxes: 330, 331, and 332.

Fig. 2

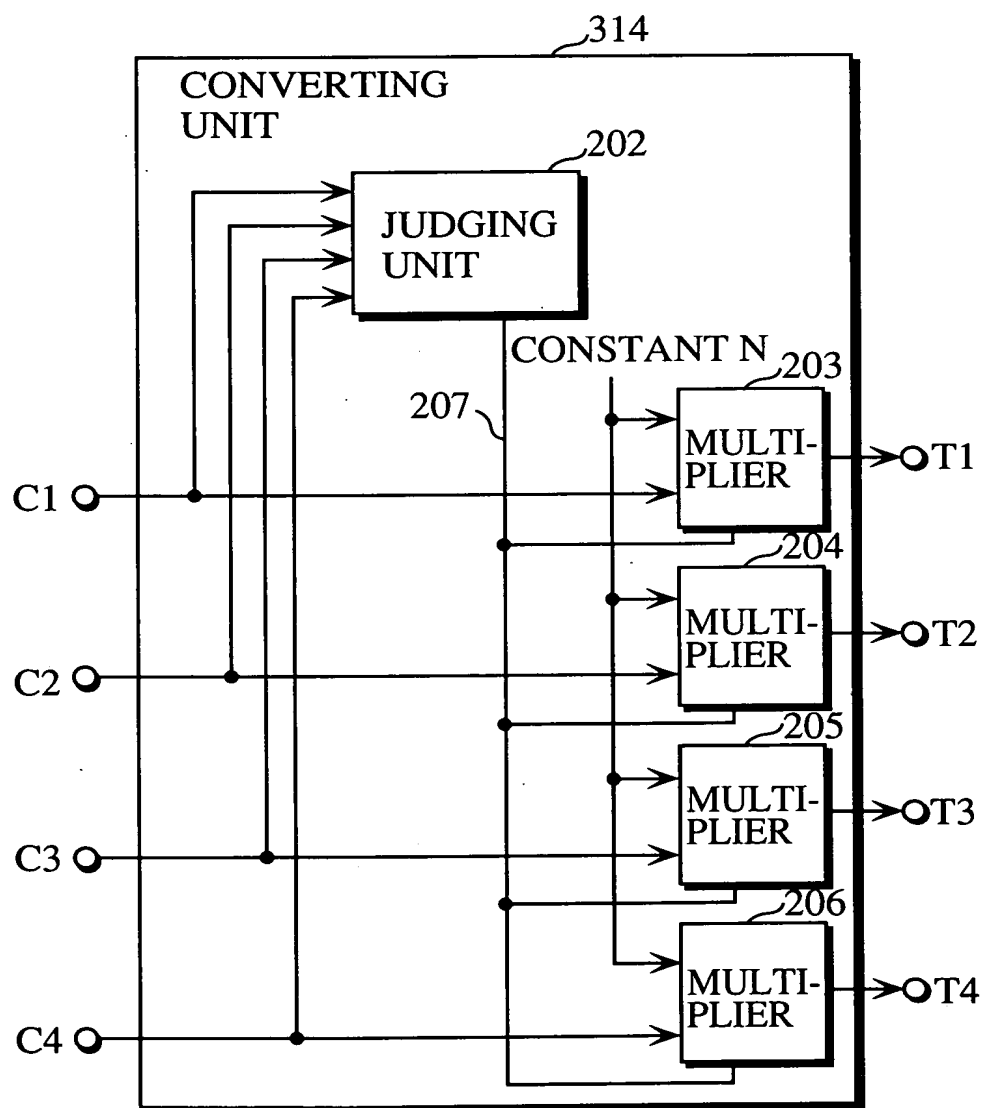


Fig. 3B

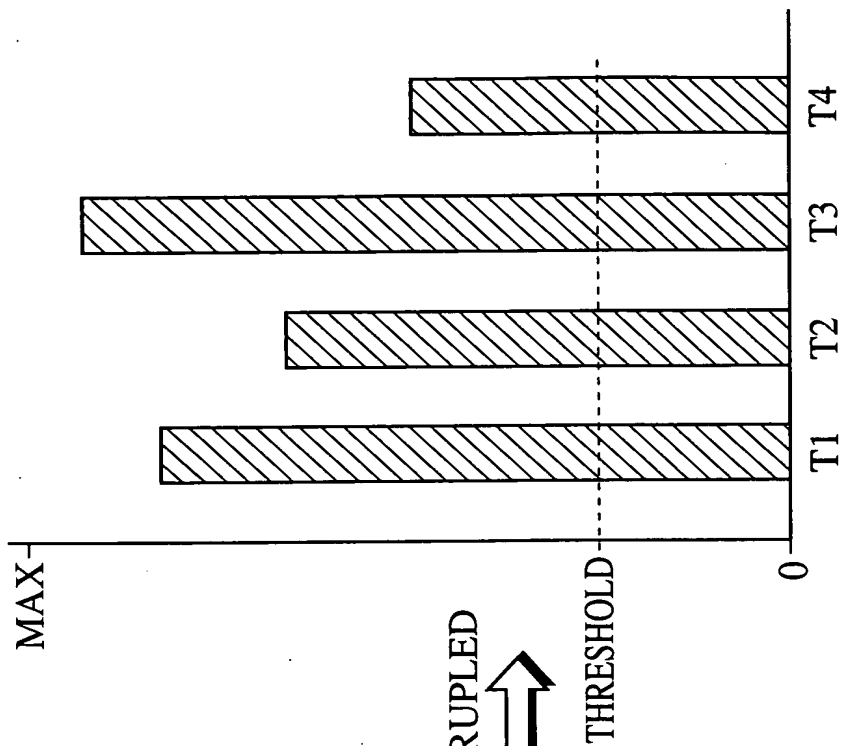
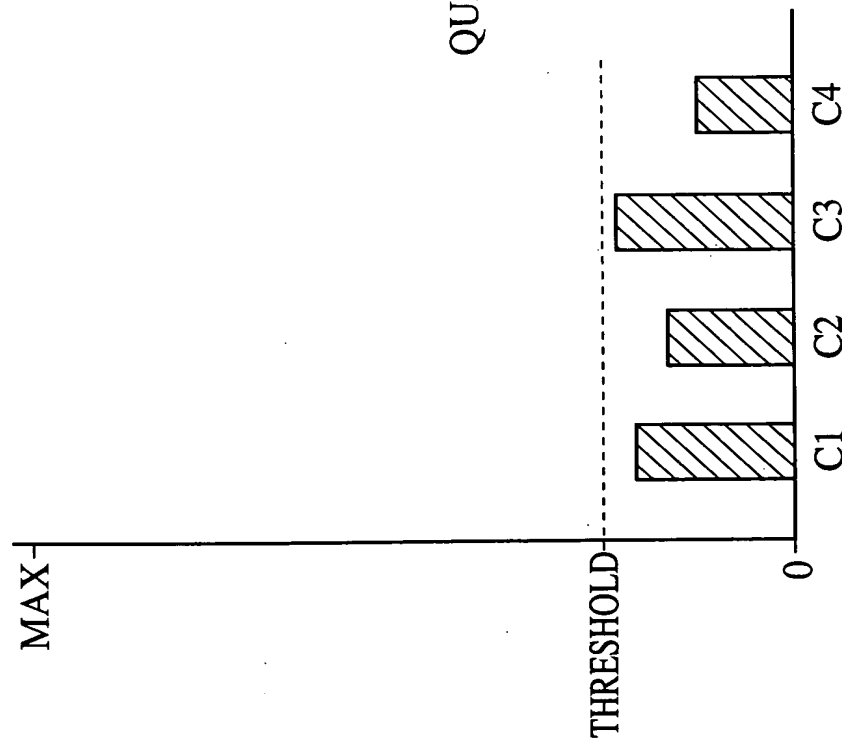


Fig. 3A



QUADRUPLED



Fig. 4

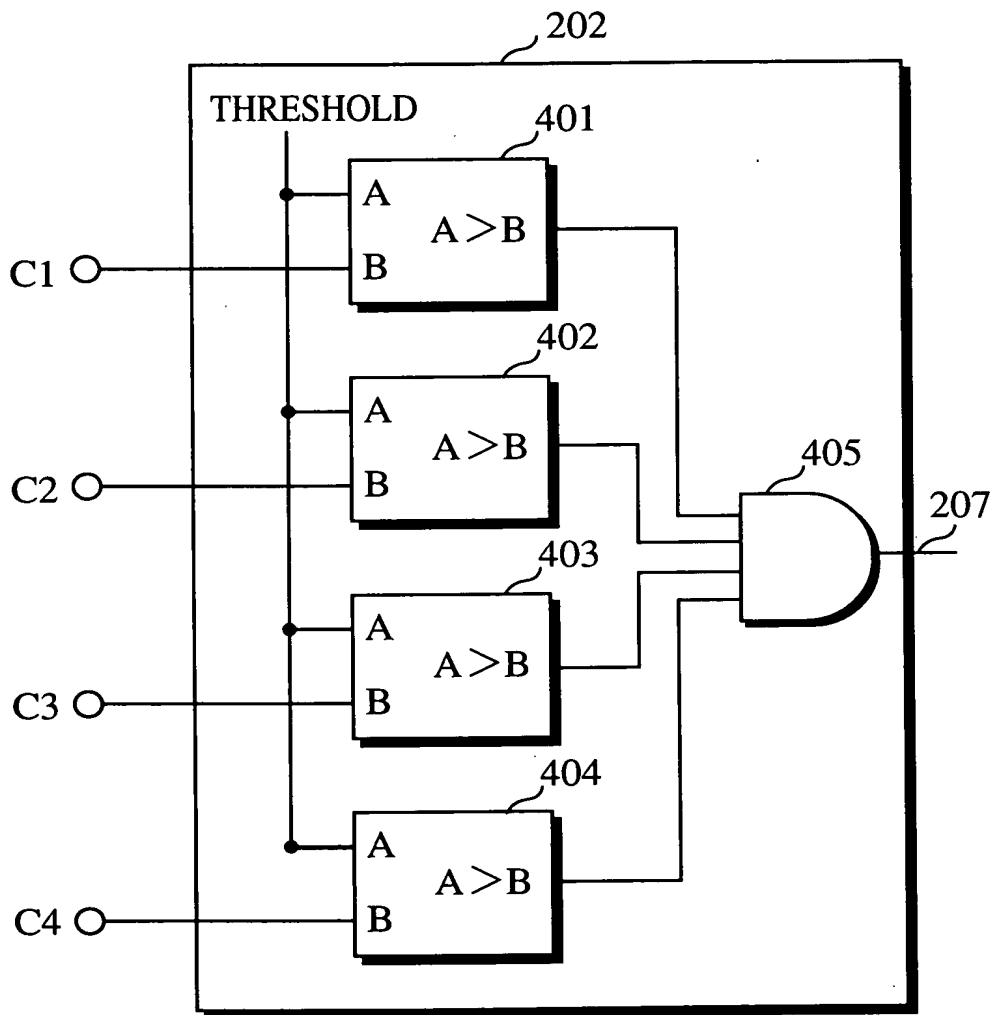


Fig. 5

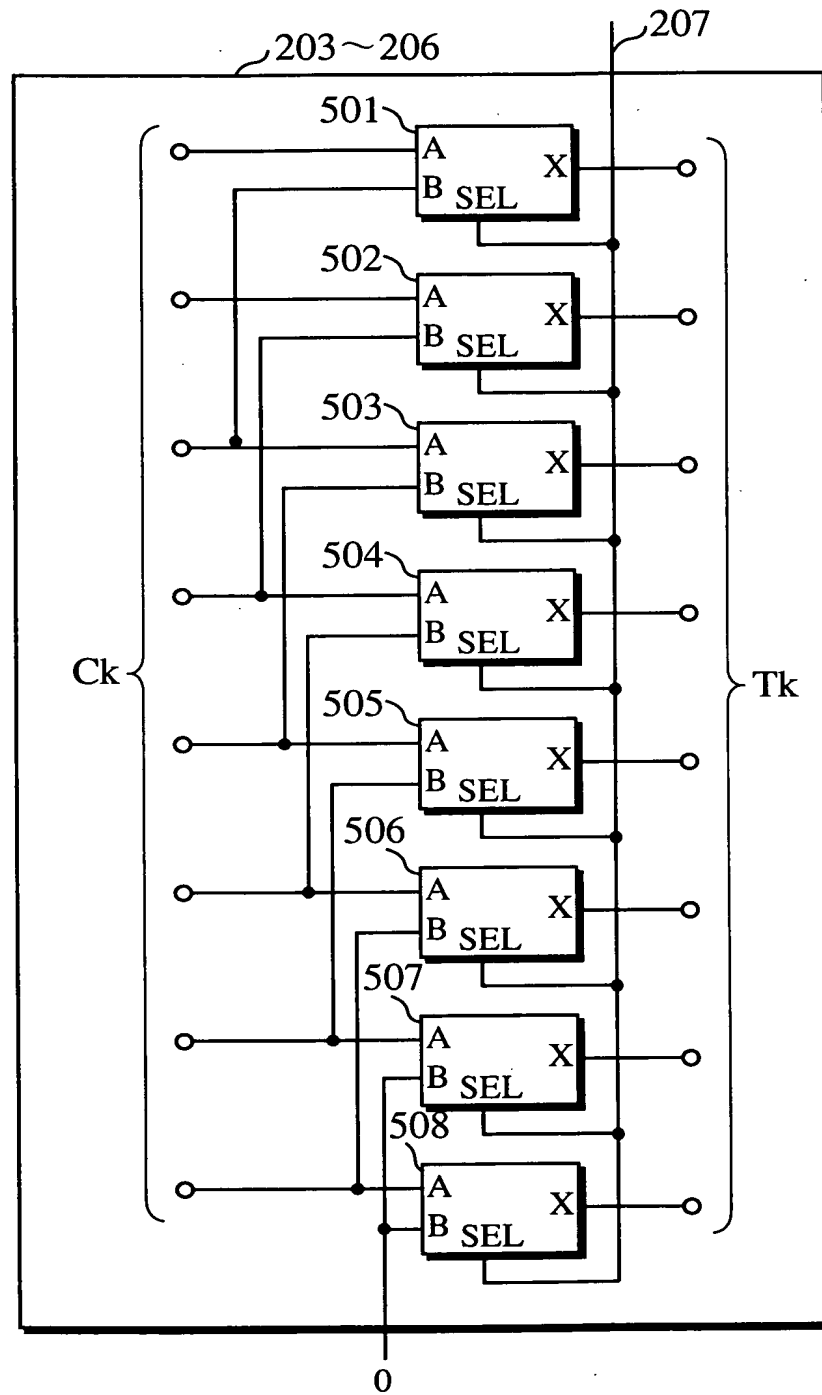


Fig. 6

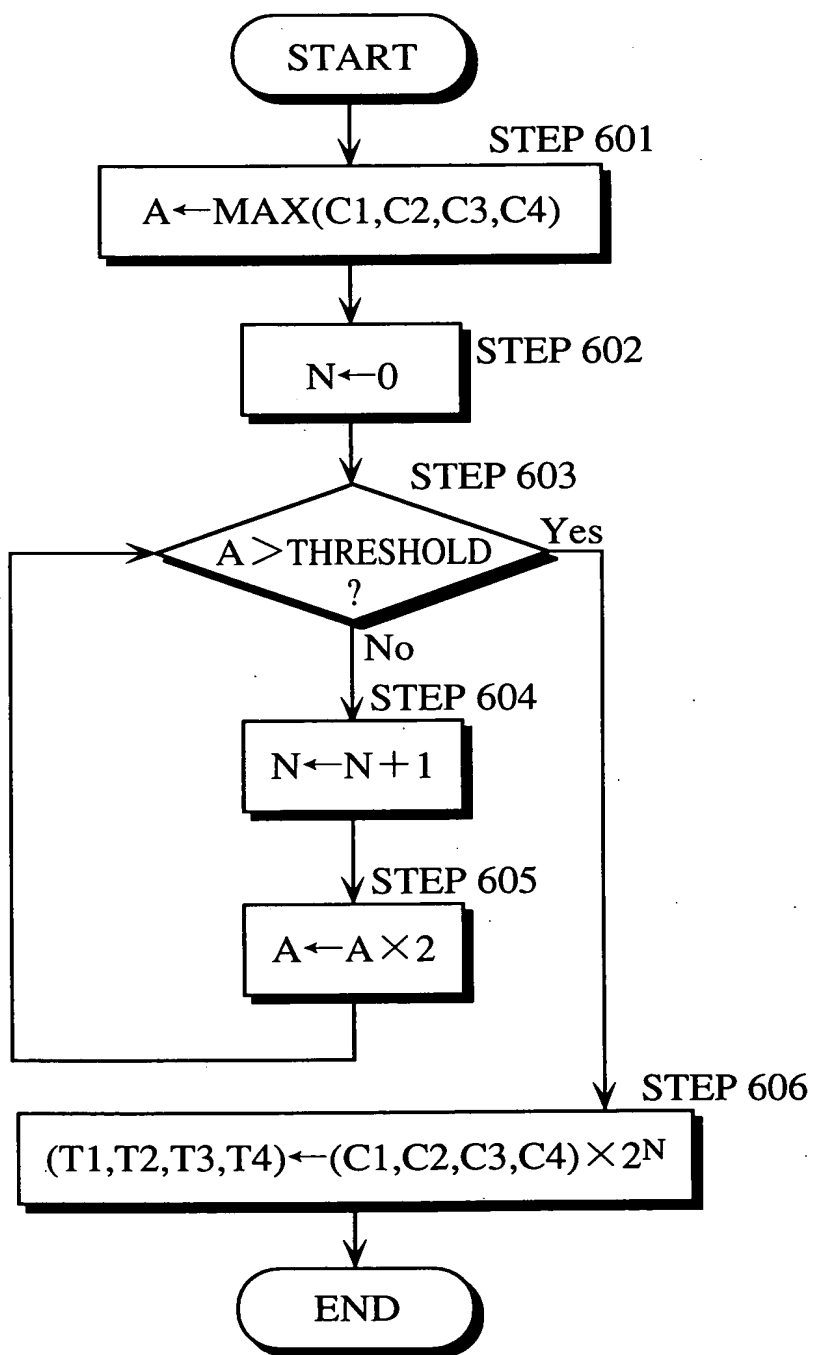
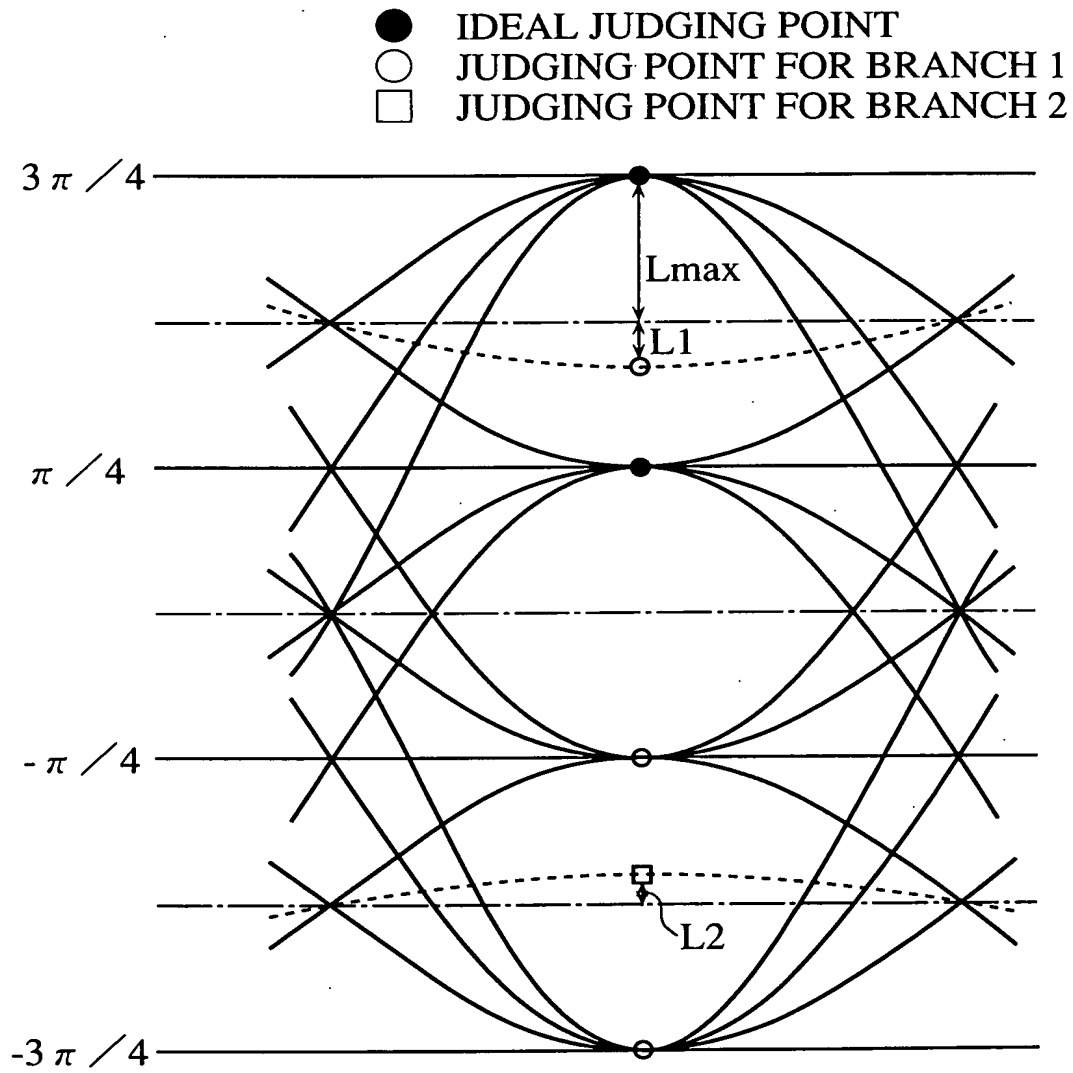


Fig. 7



Fi. 8

